PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03K 19/003 — A1

(11) International Publication Number: WO 97/40579

(43) International Publication Date: 30 October 1997 (30.10.97)

(21) International Application Number: PCT/US97/06642

(22) International Filing Date: 18 April 1997 (18.04.97)

(30) Priority Data:
635,853 22 April 1996 (22.04.96) US

(71) Applicant: UNITED TECHNOLOGIES CORPORATION [US/US]; Hamilton Standard Division, One Hamilton Road, Windsor Locks, CT 06096-1010 (US).

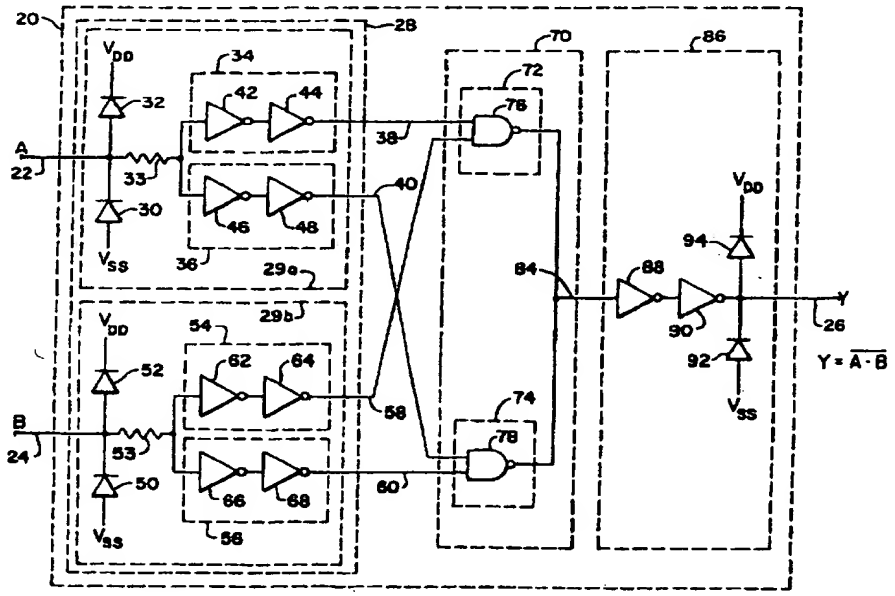
(72) Inventors: LAHEY, Michael, D.; 2075 Chapel Hills Drive, Colorado Springs, CO 80920 (US). HARRIS, Debra, S.; 2113 Winston Road, Colorado Springs, CO 80909 (US). GARDNER, Harry, N.; 1605 Bandedrock Court, Colorado Springs, CO 80919 (US). BARRY, Michael, J.; 16025 S.W. Colony Place, Tigard, OR 97224 (US).

(74) Agent: KELLY, Robert, H.; Intellectual Property Counsel, Hamilton Standard, One Hamilton Road, Windsor Locks, CT 06096-1010 (US).

(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: RADIATION RESISTANT LOGIC CIRCUIT



(57) Abstract

Apparatus for performing a selected logic function includes a first logic portion which receives one or more logic state input signals and performs the selected logic function on the input signals to provide one or more output signals, and further includes a second logic portion which receives the one or more input signals and performs the selected logic function on the input signals to provide one or more output signals, and combines each output signal from the first logic portion with the corresponding output signal from the second logic portion to provide one or more resultant logic output signals which have improved reliability in a radiation environment.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

Description

RADIATION RESISTANT LOGIC CIRCUIT

Technical Field

This invention relates to semiconductor electronic circuits and more particularly to semiconductor logic circuits.

Background Art

A single event upset (SEU) is the result of an ion transitioning through a semiconductor structure and depositing charge on a critical circuit node within that structure. In a CMOS logic circuit, this can cause an unintended switch in the logic state, creating potentially catastrophic consequences for the system. In the case of storage cells, the primary SEU problem lies in the feedback path, where amplification and feedback of noise on a critical node can permanently change the cell's logic state.

Known SEU hardening techniques for CMOS logic include the use of redundant circuit paths. Dual circuit paths provide redundancy and allow implementation of voting schemes to reduce the effect of SEUs. However, the typical voting scheme uses digital logic to recombine the redundant paths, and thereby actually provides amplification of the SEU.

Disclosure of Invention

An object of the present invention is to provide a logic circuit architecture which has higher reliability in a radiation environment.

Still another object of the present invention is to provide circuitry for a family of logic products having higher reliability in a radiation environment.

According to the present invention, apparatus for performing a selected logic function includes a first logic portion which receives one or more logic state input signals and performs the selected logic function on the logic state input signals to provide one or more output signals, and further includes a second logic portion which receives the one or more logic state input signals and performs the selected logic function on the logic state input signals to provide one or more output signals, and further combines each output signal from the first logic portion with the corresponding output signal from the second logic portion to provide one or more resultant logic output signals.

In further accord with the present invention, apparatus for performing a selected logic function includes an input section which receives one or more logic state input signals and provides a pair of buffered logic state signals for each, and further includes, a logic section having a first and second portion, each receiving one logic state signal from each of the pairs of buffered logic state signals, and each performing the selected logic function on the logic state signals received thereby to each provide one or more output signals, and each of said output signals from the first portion combined in analog fashion with a corresponding one of the output signals from the

second portion to provide one or more logic section output signals, and further includes an output section receiving each of the one or more logic section output signals and providing one or more resultant logic output signals.

The present invention provides a combinatorial logic circuit having higher reliability in a radiation environment The present invention further provides circuitry for a family of products having higher reliability in a radiation environment with little impact to the die size and no decrease in functionality.

These and other objects, features, and advantages of the present invention will become apparent in light of the following detailed description of a best mode embodiment, accompanying Drawings, and claims.

Brief Description of the Drawings

FIG. 1 is a schematic illustration of a NAND logic function, which is used in the description of the present invention;

FIG. 2 is a schematic illustration of the best mode embodiment of the present invention as used in the NAND logic function of FIG. 1;

FIG. 3 is a schematic illustration of one element used in the embodiment of Fig. 2; and

FIG. 4 is a schematic illustration of another element used in the embodiment of Fig. 2.

Best Mode for Carrying out the Invention

The apparatus of the present invention is disclosed with respect to a best mode embodiment for use in a logic circuit providing the NAND logic function represented in FIG. 1. As should be understood by those skilled in the art, the drawing figures are only schematic representations, and are not intended to portray physical details.

Referring to FIG. 1, in a prior art schematic of a selected logic device, a two input NAND circuit **20** receives logic signal A on line **22** and logic signal B on line **24**, and produces a NAND logic output signal Y on line **26**. As known, the logical operation of the NAND circuit **20** can be described by the equation Y = NOT(A•B).

Referring now to FIG. 2, in the present invention's best mode embodiment of the NAND circuit **20** of FIG. 1, logic signal A on line **22** and logic signal B on line 24 are each received by an input section **28**.

Each of the logic signals on lines 22, 24 are presented to an associated one of a pair of signal conditioning circuits 29a, 29b within the input section **28.** As described hereinafter, the signal conditioning circuits 29a, 29b are identical. The circuit 29a has a diode **30** which provides protection against logic signal A magnitudes less than the lower power supply voltage magnitude V_{SS}, and a diode **32** which provides protection against logic signal A magnitudes greater than the upper power supply voltage magnitude V_{DD}. In the best mode embodiment V_{SS} is approximately zero *(0)* volts and V_{DD} is in the range of from *4.5* to *5.5* volts. To afford the best protection,

the diodes 30, 32 are physically located as close to where the input signal on line 22 is received, as is practical. In situations where the input signal A on line 22 cannot exceed the magnitude range of the power supplies, such as where the source of logic signal A resides on the same integrated circuit as the NAND circuit 20, the two diodes 30, 32 may not be necessary.

The circuit 29a further comprises a series resistor 33 that is electrically connected between the diodes 30, 32 and the signal inputs a pair of buffer stages 34, 36. The resistor 33 provides electrostatic discharge protection (ESD) on line 22. The buffer stages 34, 36 each receive the ESD protected signal and provide a pair of buffered, redundant A signals on lines 38, 40 respectively. The pair of buffer stages 34, 36 represent independent signal paths, such that, a failure in one of the pair of buffer stages 34, 36 will not disturb the logic signal out of the other. To further this end, in the best mode embodiment, the pair of buffer stages 34, 36 are physically spaced further apart than normal so that the effect of a single ion transitioning through the semiconductor structure is less likely to cause single event upset (SEU) in both of the pair of buffer stages 34, 36.

In the best mode embodiment, the pair of the buffer stages 34, 36 provide the same logic function, non inverting buffering, and comprise logic gates of the same type, so that the pair of buffered A signals on lines 38, 40 are substantially similar to each other in logic state and timing. However, as will be obvious to those skilled in the art, one or both of the pair of buffer stages 34, 36 may provide a logic

function other than non inverting buffering, so long as suitable modifications are made to other logic, described below, in the NAND circuit **20**.

In the best mode embodiment, each of the buffer stages **34** and **36**, comprise cascaded first and second inverter **42**, **44** and **46**, **48**, respectively. The inverters are shown to be identical. The first inverters **42**, **46** buffer and invert the logic signal . The second inverters **44**, **48** restore the logic states of the pair of buffered A signals on lines **38**, **40** to that of the input signal A on line **22**.

Fig. 3 is a circuit for the inverter **42**, which comprises a P channel MOSFET **42a** and an N channel MOSFET **42b**. The input pin (IN) of the first inverter **42** is electrically connected to the gate **42c** of the P channel and the gate **42d** of the N channel MOSFETs. The source **42e** of the P channel is connected to V_{DD} and the source **42f** of the N channel is connected to V_{SS}. The drain **42g** of the P channel MOSFET is connected to the drain **42h** of the N channel which then serves as the output (OUT) for the first inverter **42**. The other inverters **44**, **46**, **48** have similar transistor level circuits to that of the first inverter **42**.

The operation of the first inverter **42** is as follows. When the signal input at IN is at a high logic state voltage, the N channel MOSFET **42b** is "on", i.e. its resistance from drain to source is low, and the P channel MOSFET **42a** is "off", i.e. its resistance from drain to source is high. At the output, this produces a low resistance to the V_{SS} supply and a high resistance to the V_{DD} supply. The result is a voltage on the output (OUT), approximately equal to V_{SS}, which

represents a low logic state. When IN is at a low logic state voltage, the P channel MOSFET **42a** is "on" and the N channel MOSFET **42b** is "off". At the output, this produces a low resistance to the V_{DD} supply and a high resistance to the V_{SS} supply. The result is a voltage on the output (OUT), approximately equal to V_{DD}, which represents a high logic state.

Referring again to FIG. **2**, the B input logic signal on line **24** is received by signal conditioning circuitry 29b which is similar to that described with respect to circuit 29a. Two diodes **50, 52** provide under voltage and over voltage protection. In situations where the input signal B on line **24** can not exceed the range of the power supplies the two diodes **50, 52** may not be necessary. A series resistor **53** is positioned after the two diodes **50, 52** to provide electrostatic discharge protection (ESD) on the input signal B on line **24**. The ESD protected input signal is then passed to a pair of buffer stages **54, 56** which provide a pair of buffered B signals on lines **58, 60** respectively. A failure in one of the pair of buffer stages **54, 56** will not disturb the logic signal out of the other. In the best mode embodiment, the pair of buffer stages **54, 56** are physically spaced further apart than normal so that the effect of a single ion is less likely to cause single event upset (SEU) in both of the pair of buffer stages **54, 56**.

In the best mode embodiment, the pair of buffer stages **54, 56** provide the same logic function, non inverting buffering, and comprise logic gates of the same type, so that the pair of buffered B signals on lines **58, 60** are substantially similar to each other in logic

state and timing. As will be obvious to those skilled in the art, one or both of the pair of buffer stages **54, 56** may provide a logic function other than non inverting buffering, so long as suitable modifications are made to other logic, described below, in the NAND circuit **20**.

In the best mode embodiment, each of the buffer stages **54** and **56**, comprise a first and second inverter **62, 64** and **66, 68**, respectively. The first inverters **62, 66** buffer and invert the input signal B on line **24**. The second inverters **64, 68** restore the logic states of the pair of buffered B signals on lines **58, 60** to that of the input signal B on line **24**. All four of these inverters **62, 64, 66, 68** have similar transistor level circuits to that of the first inverter **42**. The NAND circuit **20** further comprises a logic section **70** having a first portion **72** and a second portion **74**. The first and second portions **72, 74** each receives one signal from each of the buffered A and B signal pairs on lines 38, 40 and 58,60. The first and second portions **72, 74** represent independent signal paths, such that, a failure in one will not disturb the logic of the other. To this end, in the best mode embodiment, the portions **72, 74** are physically spaced further apart than normal so that the effect of a single ion transitioning through the semiconductor structure is less likely to cause single event upset (SEU) in both portions **72, 74**.

Each portion **72, 74** comprises the logic necessary to enable it to provide the overall logic function of the circuit, e.g. the NAND logic function of the NAND circuit **20** in the best mode embodiment. The appropriate logic depends not only on the overall logic function of the circuit, but also on the logical effect of the input section **28**

buffer stages **34**, **36**, **54**, **56** and the output section, described hereinbelow. In the best mode embodiment, the input section **28** buffer stages **34**, **36**, **54**, **56** and the output section are non inverting buffers, and therefore have no logical effect. Consequently, the logic for the first and second portions **72**, **74** of the logic section **70** each need only comprise a NAND gate **76**, **78**, or its equivalent, to provide the NAND function.

A schematic representation of the transistor level circuit for the NAND gate **76** of the first portion **72** is shown in Fig. **4**. Referring now to Fig. **4**, the NAND gate **76** has a first input **76a** which is electrically connected to the gates **76b**, **76c** of a first pair **76d** of P channel MOSFETs. The first pair **76d** of P channel MOSFETs have their sources **76e** electrically connected to V_{DD} and their drains **76f** electrically connected to the drains **76g** of a second pair **76h** of P channel MOSFETs. The sources **76i** of the second pair **76h** of P channel MOSFETs are connected to V_{DD} and the gates **76j**, **76k** are connected to the second input signal **76l**.

The drains **76f**, **76g** of both pairs **76d**, **76h** of P channel MOSFETs are further connected to the drains **76m** of a first pair **76n** of N channel MOSFETs and the output **76p** of the NAND gate **76**. The first pair **76n** of N channel MOSFETs have their gates **76q**, **76r** connected to the second input **76l**. Each of the sources **76s** of the first pair **76n** of N channel MOSFETs is connected to a different one of the drains **76t** of a second pair **76u** of N channel MOSFETs. The second pair **76u** of N channel MOSFETs have their gates **76v**, **76w**

connected to the first input 76a and their sources 76x connected to V_{SS}.

The operation of the NAND gate 76 is as follows. When both of the inputs are at a high logic state voltage, both pairs 76n, 76s of N channel MOSFETs are "on", i.e. low resistance, and both pairs 76d, 76h of P channel MOSFETs are "off", i.e. high resistance. At the output 76p, this produces a high resistance to the V_{DD} supply and a low resistance to the V_{SS} supply. The result is an output voltage of approximately V_{SS}, representing a low logic state. When one or more of the inputs 76a, 76l are at a low logic state voltage, the pair 76d, 76h of P channel MOSFETs having that input connected to its gate 76b, 76c are "on" and the pair 76n, 76s of N channel MOSFETs having that input connected to its gate are "off". At the output 76p, this produces a low resistance to the V_{DD} supply and a high resistance to the V_{SS} supply. The result is an output voltage of approximately V_{DD}, representing a high logic state.

Referring again to FIG. 2, the NAND gate 78 of the second portion 74 has a similar transistor level circuit schematic (not shown) and operation to that of the NAND gate 76 of the first portion 72. The first and second portions 72, 74 each operate on their respective input signals and produce first and second portion output signals which are summed, or combined, in analog fashion to produce a logic section output signal on line 84.. The logic section output signal on line 84 takes on the logic state corresponding to the voltage of the analog combination. This is in contrast to a combination that combines the signals by performing a logical operation on each of

their logic states.

In the best mode embodiment, the transistors in the NAND gates 76, 78 have "on" resistances in the range of from about *500* ohms to *5,000* ohms. Lower resistances are not required because the NAND gates do not to provide high magnitude output current. Accordingly, the connection should have an electrical resistance of about less than *500* ohms, preferably less than *10* ohms. In the best mode embodiment, a direct electrical connection having a resistance below *1* ohm, specifically about *.01* ohms, is used. However, those skilled in the art will recognize that other suitable transistors having other "on" resistances , and other connections having other resistances may also be used.

Normally, the transistors of both of the NAND gates **76, 78** are in similar "on" and "off" states. Consequently, the voltage contributions from the first and second portions to the logic section output signal on line 84 are both approximately V_{SS}, or both approximately V_{DD}, and the combined signal, the logic section output signal on line 84, is also approximately V_{SS}, corresponding to a logic low, or V_{DD}, corresponding to a logic high.

Statistically, only one transistor will experience SEU at a given time. Thus when an ion transitions through the semiconductor one portion **72, 74** of the logic section **70**, may experience SEU in one of the transistors in its NAND gate 76, 78. That transistor may change state from "on" to "off" or "off" to "on". However, any change in logic section output signal voltage on line 84, is small, since the output from the affected portion is combined, in analog fashion, as described above, with the output from the unaffected portion.

Consequently, the voltage effect of the SEU is reduced, or attenuated. At or below the designed ion energy level of *80* MeVcm^2/mg, there is insufficient energy in the ion to cause the logic section output signal on line 84 to transition to an incorrect logic state. Thus the logic section output signal on line 84 remains at the correct logic state throughout the SEU. The typical SEU lasts for about *20* nano seconds after which the transistor experiencing SEU returns to its prior state. Capacitance in the output portion, described hereinbelow, provides additional filtering for the small voltage changes in the logic section output signal on line **84**.

In comparison to the present invention, other approaches, which may use a voting stage, tend to amplify the effect of the SEU because they first translate the affected signal to its own logic state prior to the voting stage, and then in the voting stage, they attempt to eliminate the effect of the SEU. These other approaches also require more gates, since they require a voting stage and often require three voting signals rather than just two, as in the present invention.

It should be recognized that this approach is not a typical method for the combination of logic signals from logic gates having active pull ups and pull downs in the output stage. For example, while open collector TTL gates may be wired-ANDed, the wired-ANDing of active pull up TTL gates is prohibitive due to the high power dissipation that occurs if one gate output is high and the other gate output is low. Similarly, in ECL logic, gates may be wired-ORed but the ECL output stage only has an active pull up and does not have an active pull down. However, in the present invention, the

output of each CMOS gate does have both active pull up and active pull down.

Furthermore, unlike the TTL and ECL techniques above which seek to conserve logic gates while implementing standard logic functions, the summation approach of the present invention does not operate as a standard logic function. In fact, the summation here should not be used for combining logic signals which are not substantially similar in state and timing for the very reason that it does not provide a normal logical combination. Instead, it provides a means for combining substantially similar signals wherein a SEU failure in one of the signals does not cause failure of the combined signal.

The logic section output signal on line **84** is passed to an output section **86**. Nodal capacitance, not shown, on line **84**, provides some additional filtering for the logic section output signal. The output section **86** further comprises a pair of inverters **88, 90** for buffering of the signal. The pair of inverters **88, 90** are similar to that of the first inverter **42** of the A input signal buffer stage **34** with the exception that the transistors sizes are larger to reduce the likelihood that they themselves will experience SEU. Larger and stronger transistors are better able to resist SEU by counting the collection of charge through the substrate that is brought on by the entering ion. The pair of inverters **88, 90** are also larger to provide the desired capability for driving additional logic circuits that may be connected to the output logic signal Y on line **26**. The output section further includes a pair of diodes **92, 94** to protect against under and over voltage damage.

As with all circuitry, appropriate decoupling should be used when employing the present invention.

In the best mode embodiment, the NAND circuit **20** is implemented in CMOS technology, preferably **1.2** micro meters (um) or smaller, however, any other suitable technology may also be used. At **1.2** um the circuit is small enough in size, has relatively low power, and provides high speed operation.

In the best mode embodiment, each of the logic signals on lines **22, 24, 26** are of the type having CMOS logic levels, however, as will be obvious to those skilled in the art, the NAND logic circuit **20** may also be designed to accommodate TTL logic signals. In the preferred embodiment, this only requires threshold modifications in the input section.

Although the best mode of the present invention creates the logic section output signal on line **84** by combining the outputs from NAND gates **76, 78,** those skilled in the art will recognize that other transistor configurations may also be suitable. For example, transistor configurations to be connected may also be of the type used in inverters.

While the best mode of the present invention includes an input section, the logic section of the present invention may also be used without the input section or portions of the input section. For example, each input logic signal may be routed directly to both portions of the logic section, without passing through the input section, so long as the logic section is suitably adapted for operation with the logic levels of the input logic signals.

The present invention may also be used without the output section of the best mode embodiment. Instead, the logic section output signal may be used to drive other logic directly so long as the logic section is suitably adapted for driving such other logic.

Although disclosed with respect to a best mode embodiment for use in a NAND circuit, the present invention may be used in logic circuits of any type, including but not limited to that of OR, NOR, XOR, XNOR, inverter, AND, buffer, flip flop, line drivers and transceivers, with or without three-state outputs.

Furthermore, while the NAND circuit of the present invention has *2* inputs and *1* output, the present invention ;may be used in logic circuits having any number of inputs, e.g. N, where N is one or more, and any number of outputs, e.g. K, where K is one or more. The input section still preferably receives each of the N input signals and produces a pair of buffered signals for each. One signal from each pair of buffered signals is received by the first portion of the logic section and the other signal from each pair is received by the second portion. Each of the two logic section portions has all of the necessary logic gates for implementing the overall function. The first portion produces K first portion output signals and the second portion produces K second portion output signals. Each of the K first portion output signals is combined with the counterpart signal from the K second portion output signals to produce K logic section output signals. The K logic section output signals are passed to the output section where they are buffered to produce the K outputs for the circuit. As such, the present invention may also be used in logic

circuits of the type including but not limited to comparators, flip flops, decoders/demultiplexers, selectors/multiplexers, counters, shift registers, parity generators, adders, and memories.

Still further, although the best mode embodiment uses signal conditioning circuits that provide a pair of buffered signals and logic sections having two portions, signal conditioning circuits providing more than a pair of buffered signals and logic sections having more than two portions may also be used and similarly combined to provide even greater immunity to SEU.

While the particular invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. It is understood that, various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description without departing from the spirit of the invention, as recited in the claims appended hereto. Thus, upon understanding the present invention, one of ordinary skill in the art could employ the present invention in a variety of logic circuit applications. Those skilled in the art will know of the forms which are suitable for each application. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

What is claimed is:

Claims

1. Apparatus for performing a selected logic function on one or more logic state input signals presented thereto to provide one or more resultant logic output signals, comprising:

a first logic portion, receiving each logic state input signal and performing the selected logic function on the logic state input signals to provide one or more output signals; and

a second logic portion, receiving each logic state input signal and performing the selected logic function on the logic state input signals to provide one or more output signals, and each of said output signals from said second logic portion combined in analog fashion with a corresponding one of said output signals from said first logic portion to provide the one or more resultant logic output signals.

2. The apparatus of claim 1 wherein said output signals of said first and second logic portions are provided by logic gates having outputs with active pull ups and active pull downs.

3. The apparatus of claim 1 wherein said first and second logic portions comprise CMOS technology.

4. The apparatus of claim 1 wherein said combination in analog fashion of said first logic portion output signals and said second logic

portion output signals comprises an electrical connection having a resistance of about less than 500 ohms.

5. The apparatus of claim **1** wherein said first logic portion and said second logic portion comprise identical logic circuitry.

6. The apparatus of claim **1** wherein said first logic portion and said second logic portion are physically separated to prevent an ion from causing SEU in both portions.

7. The apparatus of claim **1** wherein said combination in analog fashion of said first logic portion output signals and said second logic portion output signals to produce the one or more resultant output signals is immune to SEU at ion energy levels of up to and including *80* $MeVcm^2/mg$.

8. The apparatus of claim **1** wherein said combination in analog fashion of said first logic portion output signals and said second logic portion output signals comprises a direct electrical connection having a resistance of about less than 1 ohm.

9. Apparatus for performing a selected logic function on one or more logic state input signals presented thereto to provide one or more resultant logic output signals, comprising:

an input section having a signal conditioning circuit for each of the logic state input signals, for providing for each of the logic state input signals, a pair of buffered logic state signals;

a logic section having a first and second portion, each receiving one logic state signal from each of said pairs of buffered logic state signals, and each performing the selected logic function on said logic state signals received thereby to each provide one or more output signals, and each of said output signals from said first portion combined in analog fashion with a corresponding one of said output signals from said second portion to provide one or more logic section output signals; and

an output section receiving each of said one or more logic section output signals and providing the one or more resultant logic output signals.

10. The apparatus of claim **9** wherein said output signals of said first and second portions of said logic section are provided by logic gates having outputs with active pull ups and active pull downs.

11. The apparatus of claim **9** wherein said first and said second portions of said logic section comprise CMOS technology.

12. The apparatus of claim **9** wherein said combination in analog fashion of said first portion output signals and said second portion

output signals comprises an electrical connection having a resistance of about less than 500 ohms.

13. The apparatus of claim 9 wherein said first portion and said second portion of said logic section comprise identical logic circuitry.

14. The apparatus of claim 9 wherein said first portion of said logic section and said second portion of said logic section are physically separated to prevent the an ion from causing SEU in both portions.

15. The apparatus of claim 9 wherein said output section comprises circuitry that is immune to SEU at ion energy levels of up to and including *80* $MeVcm^2/mg$.

16. The apparatus of claim 9 wherein said one or more logic section output signals are immune to SEU at ion energy levels of up to and including *80* $MeVcm^2/mg$.

17. The apparatus of claim 9 wherein said input section, said logic section, and said output section are on the same integrated circuit.

18. The apparatus of claim 9 wherein said input section comprises, for each of the N input signals, a pair of identical buffer stages that produce said pair of buffered signals.

19. The apparatus of claim 9 wherein for each of said pair of buffer stages, one of said pair of buffer stages is physically separated from the other of said pair of buffer stages to prevent an ion from causing SEU in both buffer stages.

20. The apparatus of claim 9 wherein said combination in analog fashion of said first portion output signals and said second portion output signals comprises a direct electrical connection having a resistance of about less than 1 ohm.

21. The method for combining first and second logic signals, each having both active pull and active pull down, to produce an output logic signal comprising the step of:

summing the first and second logic signals in analog fashion to produce an output logic signal.

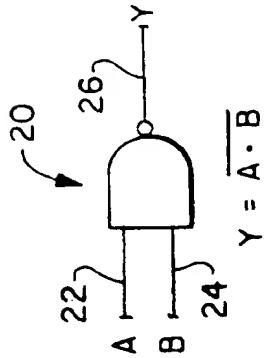


FIG. 1
PRIOR ART

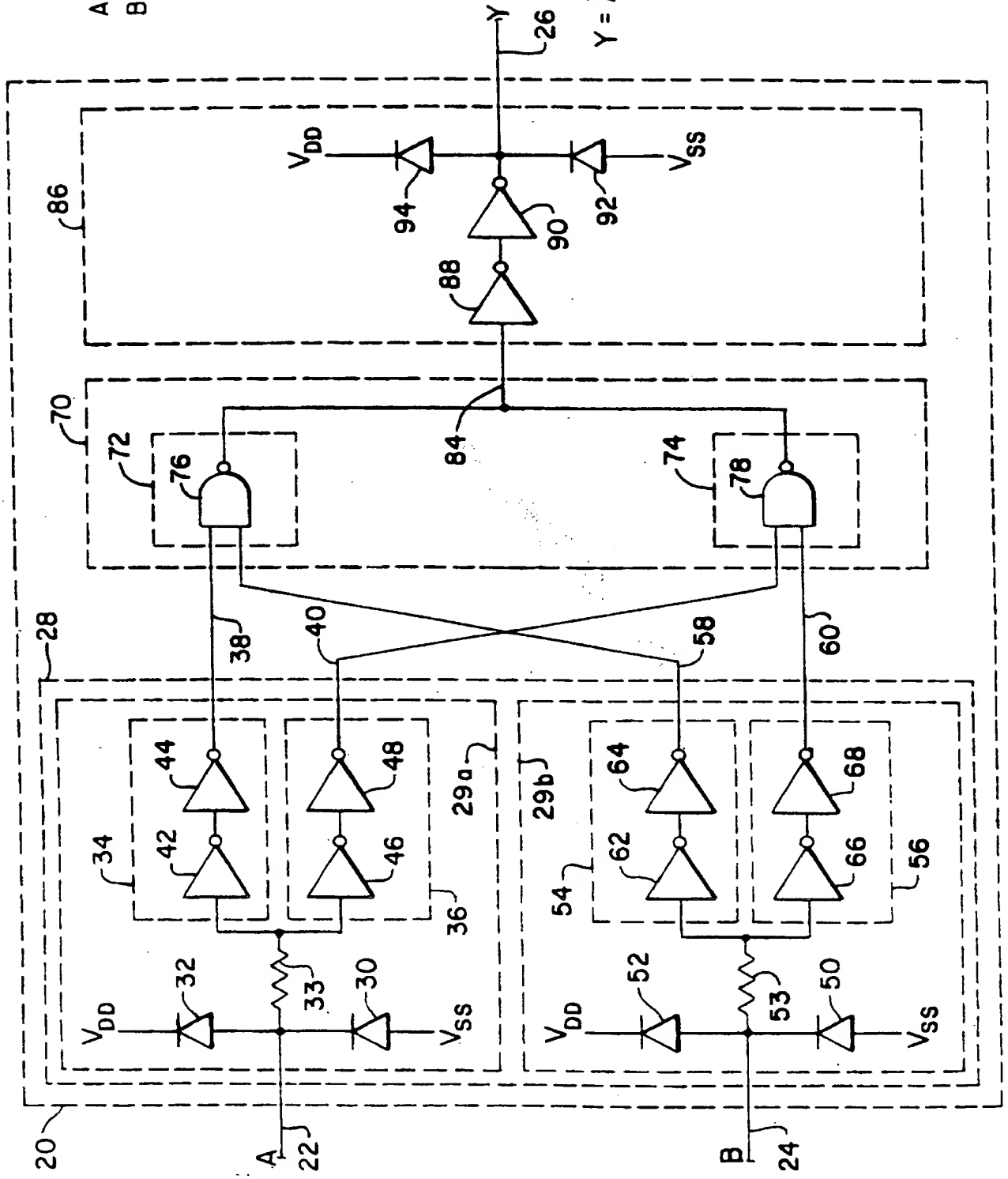


FIG. 2

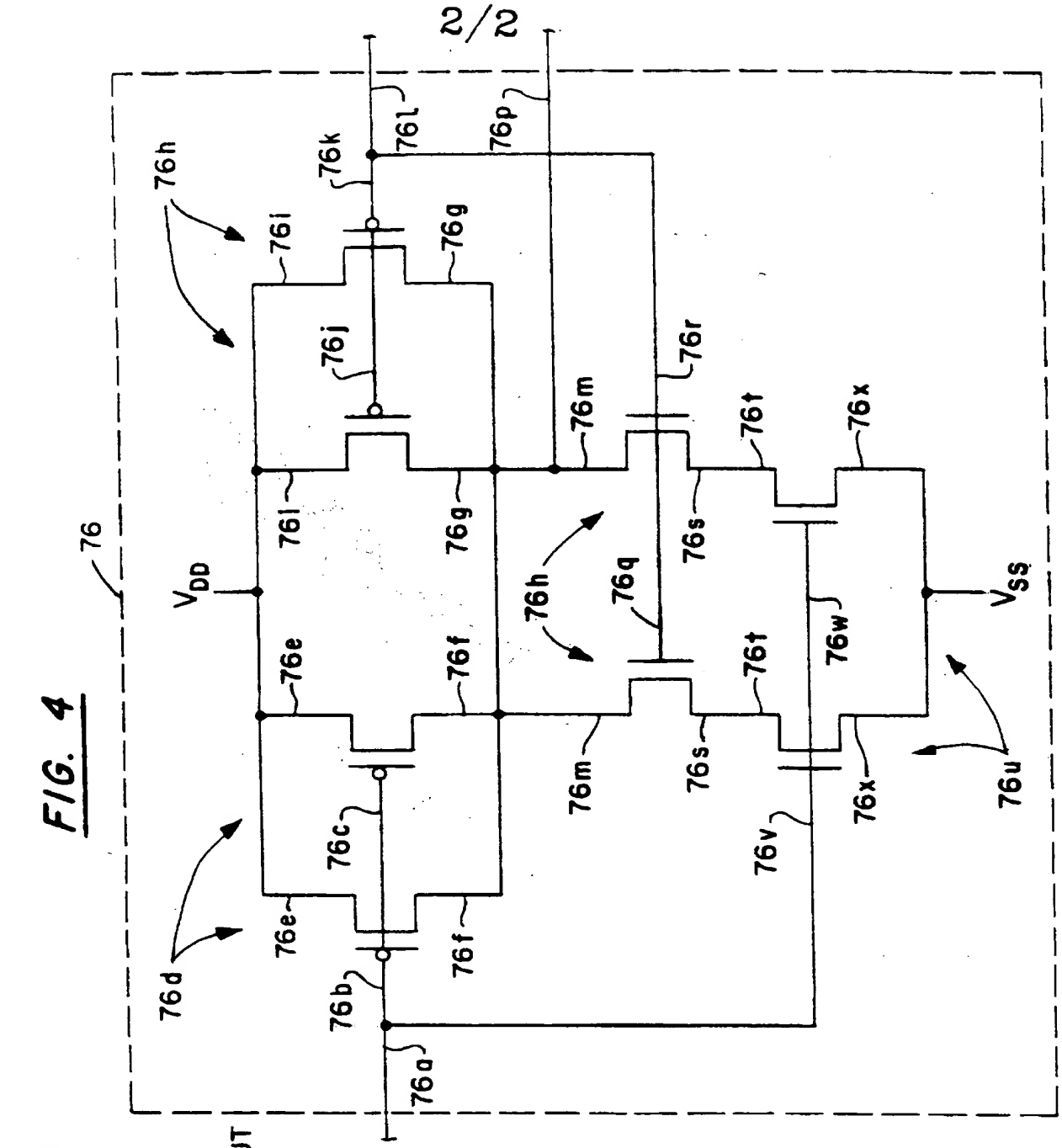

76
76h
76i
76k
76l
76p
76g
76j
76r
76m
76t
76x
76l
76g
76s
V_{DD}
76h
76q
V_{SS}
76e
76f
76t
76w
76m
76s
76x
76u
76c
76v
76d
76e
76f
76b
76a

FIG. 4

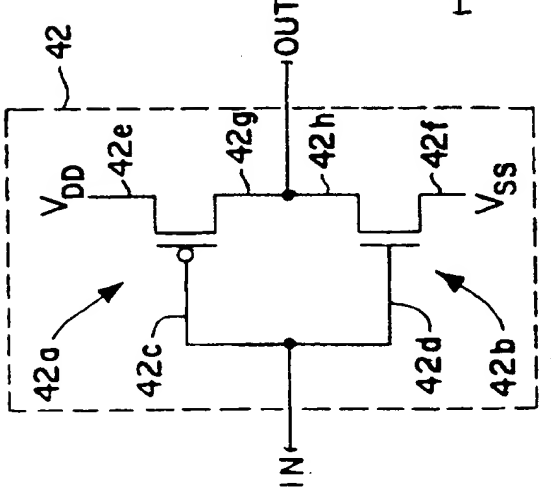

42
OUT
V_{DD}
42e
42g
42h
42f
V_{SS}
42a
42c
42d
42b
IN

FIG. 3

INTERNATIONAL SEARCH REPORT

Interna al Application No
PCT/US 97/06642

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03K19/003

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 285 789 A (IBM) 12 October 1988 see the whole document	1,9,21
A	US 5 418 473 A (CANARIS JOHN) 23 May 1995 see abstract	1,9,21
A	US 4 709 166 A (BANKER DENNIS C ET AL) 24 November 1987 see column 7; figure 3	1,9,21
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 30, no. 9, February 1988, ARMONK, US, pages 180-182, XP002038940 "Circuit using CMOS that has Redundant Duality" see the whole document	1,9,21

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
27 August 1997	08.09.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Jepsen, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Intern: al Application No
PCT/US 97/06642

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 229 (E-273), 20 October 1984 & JP 59 108422 A (NIPPON DENKI KK), 22 June 1984, see abstract	
A	IEEE TRANSACTIONS ON COMPUTERS, vol. 38, no. 1, January 1989, pages 15-29, XP000023247 BARBOUR A E ET AL: "A GENERAL, CONSTRUCTIVE APPROACH TO FAULT-TOLERANT DESIGN USING REDUNDANCY" see the whole document	
A	FR 2 386 199 A (BAILEY CONTROLE) 27 October 1978 see the whole document	
P,X	US 5 600 260 A (LAMACCHIA MICHAEL P ET AL) 4 February 1997 see the whole document	1-21

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interna l Application No
PCT/US 97/06642

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0285789 A	12-10-88	US 4829198 A	09-05-89
		CA 1278349 A	27-12-90
		DE 3854012 D	27-07-95
		DE 3854012 T	15-02-96
		JP 1848356 C	07-06-94
		JP 63263826 A	31-10-88
US 5418473 A	23-05-95	NONE	
US 4709166 A	24-11-87	DE 3750316 D	08-09-94
		DE 3750316 T	09-03-95
		EP 0250752 A	07-01-88
		JP 6105874 B	21-12-94
		JP 62274921 A	28-11-87
FR 2386199 A	27-10-78	DE 2814031 A	12-10-78
		US 4215340 A	29-07-80
US 5600260 A	04-02-97	NONE	